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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,351	02/26/2004	Ignazio Martines	61181-00013USPX	9082

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EXAMINER	
NGUYEN, NAM THANH	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 12/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/789,351	MARTINES ET AL.	
	Examiner	Art Unit	
	Nam T. Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-10,12-20,22 and 23* is/are rejected.

7)☒ Claim(s) *3,11 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *EAST search*.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The terminology "for example" makes the scope of the claim indefinite because it is not a positive limitation and it does not constitute a limitation in any patentable sense.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 4-5, 6-10, 12-13, 15-20 and 22-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Micheloni et al (US Pat. No. 6,603,681)

Regarding claim 1, a voltage regulation system (13, figure 7) for multiword programming (the memory device of Micheline et al is a multi level memory cell) in a non volatile memory, for example of the Flash type, with low circuit area occupation, wherein the memory comprises at least a memory cell matrix organized in cell rows and columns (see figure 3 for the array with row and column of cells) and with corresponding

circuits responsible for addressing, decoding (row and column decoder) reading , writing (see claim 4) and erasing the memory cell content, each cell having a drain (D in figure 7) terminal connected to a matrix column and biased in the programming step with a predetermined voltage value by a program load circuit (14 and HWSW1-HWSW4 of Fig. 7) associated with each matrix column, the system further including, in parallel with each program load circuit (as stated above), a conduction-to-ground path (when transistor YN is ON, there would be a conduction to ground through CPAR2) enabled by a controlled active element (transistor YN).

Regarding claim 2, the controlled active element is a pass transistor (YN) receiving on the control terminal thereof a first enabling signal (the output of HWSW3).

Regarding claims 4 and 5, since the conduction to ground path (from XY to ground) of Micheloni et al is intended to be used as a practical substitute, then this conduction path would be considered as a redundant current path or a dummy current path.

Regarding claim 6, a non-volatile memory cell (CM of fig. 7) are coupled to a bit line (the line that connects to VD) and a word line (WORD LINE); and a selectively actuated conduction to ground path coupled to the bit line (when YO and YN are ON, the bit line is conducted to ground path).

Regarding claim 7, the non-volatile memory cell (CM) comprises a floating gate transistor (CM is a floating gate transistor) having its drain terminal (VD) connected to the bit line and its gate connected to the word line (WORD LINE).

Regarding claim 8, a bit line biasing circuit (YN & YO) coupled to the bit line, the selectively actuated conduction to ground path (the line from the node of XY to ground through capacitor CPAR2) being connected in parallel with the bit line biasing circuit (the line from YN to the node VD).

Regarding claim 9, the selectively actuated conduction to ground path (see explanation above) is coupled to the bit line through at least a column decoding circuit (12).

Regarding claim 10, the selectively actuated conduction to ground path (see explanation above) is coupled to the bit line (the line from drain D of CM) through at least a bit line biasing circuit (YN & YO)

Regarding claim 12, figure 7 of non-volatile memory, comprising: a memory matrix including a plurality of memory cells arranged in columns (SECTOR, figure 3), each associated with a bit line (the line between drain of CM and node D), and rows, each associated with a word line (WORD LINE); a column programming circuit (HWSW1-HWSW4) coupled between a programming voltage source (VPD) and each

bit line and activated in response to a first control signal (VPCY); and a bypass path circuit (YN, XY, and CPAR2)for each bit line and coupled between the programming voltage source (VPD) and ground and activated in response to a second control signal (VPCY).

Regarding claim 13, each memory cell comprises a floating gate transistor (CM) having its drain terminal (at node VD) connected to the bit line (the connection between drain of CM and VD) and its gate connected to the word line (see the rejection applied to claim 7).

Regarding claim 15, the memory includes a column decoding circuit (12, figure 7) for each column.

Regarding claim 16, the bypass path circuit comprises a pass transistor (YN, figure 7) for each column coupled between the programming voltage source (VPD) and ground.

Regarding claim 17, a voltage regulation system for a non volatile memory including a memory cell matrix organized in cell rows and columns (SECTOR, figure 3), comprising: a program load circuit (HWSW1-HWSW4) for each matrix column that biases each memory cell in a selected matrix column with a predetermined voltage value (VPD) during a programming operation; and a conduction-to-ground path (the

path through XY and CPAR2) for each matrix column, each path being enabled when its associated matrix column is not selected during the programming operation.

Regarding claim 18, each memory cell comprises a floating gate transistor (transistor CM is a floating gate transistor) having its drain (at node VD) terminal connected to a bit line for a column and its gate connected to a word line (WORD LINE) for a row.

Regarding claim 19, the system for a nonvolatile memory includes a column decoding circuit (12, figure 7) for each column.

Regarding claim 20, the conduction to ground path includes a controlled active element comprising a pass transistor (YN, figure 7) receiving on a control terminal thereof a first enabling signal (the input signal applied to transistor YN).

Regarding claim 22, the conduction-to-ground path is a redundant current path for the program load circuit (see the rejection applied to claim 4).

Regarding claim 23, the conduction-to-ground path is a dummy current path for the program load circuit (see the rejection applied to claim 5).

Allowable Subject Matter

4. Claims 3, 11, 14 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance:

There is no teaching or suggestion in the prior art to:

"the first enabling signal is complementary to a second enabling signal applied to the corresponding program load circuit" as claimed in the dependent claims 3 and 21; or

"the bit line biasing circuit and the selectively actuated conduction to ground path are oppositely activated" as claimed in the dependent claim 11; or

"the first and second control signals are complementary" as claimed in the dependent claim 14; or

Conclusion

5. The following prior art, which is considered pertinent to applicant's disclosure although not relied upon, includes:

Micheloni et al. (Pub. No.: US 2004/0170061) or Micheloni et al. (Pub. No.: US 2004/0170062) disclose a semiconductor memory device including a biasing circuit similar to that of the present application, but fail to disclose the claimed limitations as described above.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nam T. Nguyen whose telephone number is (571) 272-1878. The examiner can normally be reached on 8 am to 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nam T Nguyen
Examiner
Art Unit 2824

1/12/05

ANH PHUNG
PRIMARY EXAMINER